CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

IN THE CLAIMS

1. (Currently Amended) A transceiver for processing high data rate serial data, comprising:

first clock data recovery circuitry for receiving first serial data and recovering a first recovered clock from the first serial data;

a second clock data recovery circuitry for receiving second serial data and recovering a second recovered clock from the second serial data;

wherein the transceiver provides the first recovered clock, the second recovered clock, a reference clock, the first serial data and the second serial data to a circuit portion of the transceiver; and

wherein the circuit portion ~~uses one of~~ chooses among the first recovered clock, the second recovered clock and the reference clock for subsequent processing of one of the first serial data and the second serial data.

2. (Canceled)

3. (Original) The transceiver of claim 1 further comprising delay locked loop circuitry for receiving second serial data and produces a second recovered clock from the second serial data, wherein the transceiver provides the second serial data to the circuit portion and wherein the circuit portion uses one of the first recovered clock, the second recovered clock and the reference clock for subsequent processing of one of the first and second serial data.

4. (Previously presented) The transceiver of claim 1 wherein the first serial data is an receive serial bit stream.

5. (Original) The transceiver of claim 1 wherein the circuit portion comprises a portion of a programmable logic fabric.

6. (Currently Amended) A transceiver for processing high data rate serial data, comprising:

first circuitry for receiving first serial data and recovering a first recovered clock based on the first serial data, wherein the first circuitry provides the first recovered clock to a first clock based functionality; and

second circuitry for generating and providing a reference clock to a second clock based functionality;

third circuitry for receiving second serial data and recovering a second recovered clock based on the second serial data, wherein the third circuitry provides the second recovered clock to a third clock based functionality; and

wherein the first, ~~and~~ second and third clock based functionalities concurrently perform processing functions ~~using~~ by choosing among the first recovered clock, the second recovered clock, and the reference clock, respectively.

7. (Canceled)

8. (Currently Amended) A transceiver comprising:

circuitry for receiving a plurality of input serial data streams;

clock data recovery circuitry for recovering a corresponding plurality of recovered clocks based on the plurality of input serial data streams;

circuitry for providing a reference clock; and

logic for selecting from the plurality of input serial data streams and for providing at least one outgoing serial data stream to an outgoing transmit block;

wherein the logic provides each received input serial data stream of the plurality of input serial data streams to the outgoing transmit block ~~based upon~~ by choosing among each corresponding recovered clock of the plurality of corresponding recovered clocks ~~or~~ and said reference clock.

9. (Previously presented) The transceiver of claim 8 wherein the outgoing transmit block is one of a programmable transmit physical media attachment (PMA) module and a transmitter port.

10. (Currently Amended) An integrated circuit, comprising:

at least one clock recovery circuitry coupled to receive a high data rate input data stream, wherein the clock recovery circuitry recovers a plurality of recovered ~~clock~~ clocks based on the high data rate input data stream; and

a programmable logic fabric portion wherein the programmable logic fabric portion performs subsequent processing ~~based on one of~~ by choosing among the recovered ~~clock~~ clocks and a reference clock.

11. (Currently Amended) The integrated circuit of claim 10 wherein the high data rate input data stream is received according to a first protocol and is converted to a second protocol by the programmable logic fabric portion based on one of said plurality of ~~the~~ recovered ~~clock~~ clocks.

12. (Currently Amended) The integrated circuit of claim 11 further comprising transmit circuitry coupled to receive the converted high rate input data stream in the second protocol, wherein the programmable logic fabric portion provides the converted high data rate input data stream in the second protocol based on one of said plurality of ~~the~~ recovered ~~clock~~ clocks.

13. (Currently Amended) The integrated circuit of claim 11 ~~further comprising~~ wherein said at least one clock recovery circuitry comprises a second clock recovery circuit for recovering a second recovered clock based on an I/O serial data stream.

14. (Currently Amended) A method of processing high data rate serial data, comprising:

receiving a high data rate input data stream;

recovering a first recovered clock based on the high data rate input data stream;

recovering a second recovered clock based on a transmitter clock;

providing the first and second recovered ~~clock~~ clocks to a programmable logic fabric portion; and

performing subsequent processing in the programmable logic fabric portion ~~based on~~ by choosing among the recovered ~~clock~~ clocks, wherein the high data rate input data stream is received according to a first protocol.

15. (Original) The method of claim 14 wherein the high data rate input data stream is received according to a first protocol.

16. (Currently Amended) The method of claim 15 wherein the high data rate input data stream is converted to a second protocol based on the first recovered clock.

17. (Canceled)

18. (Currently Amended) The method of claim [[17]] 16 further comprising transmitting the converted high data rate input data stream in the second protocol based on the second recovered clock.

19. (Original) A method of processing high data rate serial data, comprising:

receiving a first serial bit stream and recovering a first recovered clock from the first serial bit stream;

receiving a second serial bit stream and recovering a second recovered clock from the second serial bit stream;

providing the first and second recovered clocks and a reference clock to a circuit portion; and

within the circuit portion, choosing among the first and second recovered clocks and the reference clock for subsequent processing.

20. (Previously presented) The method of claim 19 wherein the first serial bit stream is an receive serial bit stream.

21. (Previously presented) The method of claim 19 wherein the second serial bit stream is a transmit serial bit stream.

22. (Currently Amended) A method of clock management in a processing block, comprising:

receiving a first data stream and recovering a first clock based on the first data stream;

providing the first clock to a first circuit portion;

receiving a second data stream and recovering a second clock based on the second data stream;

providing the second clock to a second circuit portion;

providing a reference clock to a third circuit portion; and

concurrently performing processing functions in the processing block ~~using~~ by choosing among the first and second clocks and the reference clock.

23. (Currently Amended) A method for a receiving and transmitting data, comprising:

receiving a plurality of input data streams;

recovering a corresponding plurality of clocks based on the plurality of input data streams;

determining at least one output port for providing outgoing data streams; and

providing each input data stream of the plurality of input data streams to the at least one output port ~~based upon~~ by choosing among each corresponding recovered clock of the corresponding plurality of recovered clocks;

wherein the at least one output port comprises a number of output ports that corresponds to a number of input data streams of the plurality of input data streams, and wherein the method further comprises determining, for each input data stream of the plurality of input data streams, an output port and providing each input data stream

of the plurality of input data streams to the determined output ports based upon each corresponding chosen recovered clock of the corresponding plurality of recovered clocks.

24. (Canceled)